A NOVEL PROCESSOR HAVING SHIFT OPERATIONS

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Cited documents:

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Abstract of **WO9617289**

The processor (109) includes a decoder (202) being coupled to receive a control signal (207). The control signal has a first source address, a second source address, a destination address, and an operation field. The first source address corresponds to a first location. The second source address corresponds to a second location. The destination address corresponds to a third location. The operation field indicates that a type of packed data shift operation is to be performed. The processor further includes a circuit (203) being coupled to the decoder. The circuit is for shifting a first packed data being stored at the first location by a value being stored at the second location. The circuit is further for communicating a corresponding result packed data to the third location.